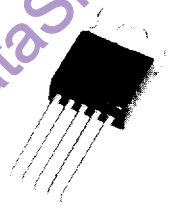
LAS-8500P
LAS-8501P

3 AMP, 40V HALF BRIDGE INTERFACE DRIVERS



FEATURES

- 6A peak source & sink current
- TTL, NMOS & CMOS compatible
- Latching thermal shutdown
- Under voltage lockout
- Input logic deadband
- 500 KHz operation

DESCRIPTION

The LAS 8500P, 8501P half bridge interface drivers are monolithic integrated circuits, designed to interface logic with high current, inductive or capacitive loads. The LAS 8500P, 8501P are designed to drive relays, solenoids, lamps and motors in half-bridge or full-bridge configuration.

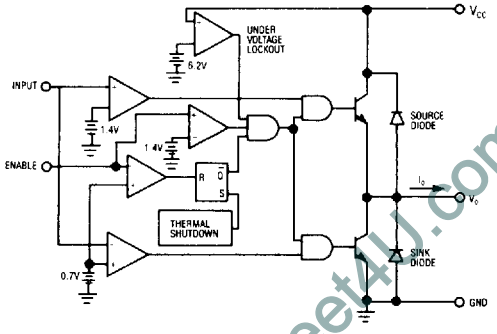
The LAS 8500P, 8501P feature a three state push-pull output, 3A of continuous current, under voltage lockout, and thermal shutdown protection. The state of the output is controlled by two logic pins and an internal thermal latch. Normally the output is controlled by two logic pins. The onset of thermal shutdown overrides the input logic and sets the output to the off state, preventing source and sink operation.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MAXIMUM	UNITS
Supply Voltage	V_{CC}	40	Volts
Input Voltage	V_{IN}	40	Volts
Enable Voltage	V_E	40	Volts
Output Current Peak Continuous	I_O	 6 3	Amps
Diode Current Peak Continuous	I_D	 5 3	Amps
Power Dissipation at T_C = 65°C[1]	P_D	15	Watts
Thermal Resistance Junction to Case[2]	θ_{JC}	4	°C/W
Operating Junction and Storage Temperature Range	T_J T_{STG}	– 25 to 125	°C
Lead Temperature (Soldering, 10 Seconds)	T_{LEAD}	260	°C

(1) For operation above T_C = 65°C, derate at 250mW/°C.
(2) Thermal Resistance Junction to Ambient, θ_{JA}, is typically 70°C/W.

BLOCK DIAGRAM



The LAS 8500P has a complementary device labeled LAS 8501P which has an inverter on the input pin. This device is useful in simplifying full bridge operation. The LAS 8500P, 8501P are available in a 5 pin TO-220 plastic package.

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ELECTRICAL CHARACTERISTICS

Test conditions are as follows: V_{CC} = 7V to 40V, I_O = 0A, T_J = 25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
INPUT CHARACTERISTICS						
Input Logic Level	V_{IN}					
"Low"			−0.3		0.5	Volts
"High"			2.0		40	Volts
Input Current	I_{IN}					
"Low"		V_{IN} = 0.5V		12	40	µA
"High"		V_{IN} = 2.4V		0.5	2.0	µA
Enable Logic Level	V_E					
"Low"			−0.3		0.5	Volts
"High"			2.0		40	Volts
Enable Current	I_E					
Enable		V_E = 2.4V		2.5	5.0	µA
Inhibit		V_E = 0.5V		6	20	µA
OUTPUT CHARACTERISTICS						
Output Voltage Saturation						
"Sink"		I_O = −3A		1.6	2.0	Volts
"Source"		I_O = 3A		2.3	3.0	Volts
Diode Voltage Saturation						
"Sink'		I_O = 3A		2.0	2.4	Volts
"Source"		I_O = 3A		1.8	2.2	Volts
Output Leakage Current	I_L			0.8	5.0	mA
Quiescent Current	I_Q					
"Sink"				14	25	mA
"Source"				20	35	
Undervoltage Lockout			5.5		7.0	Volts
Thermal Shutdown				150		°C

SWITCHING CHARACTERISTICS[1]

Test Conditions			Typical				
Input	Enable	T_J	t_d	t_r	t_s	t_f	Units
Pulsed	5V	25°c	140	60	580	100	ns
5V	Pulsed	25°C	180	70	300	N/A	ns
0V	Pulsed	25°C	110	N/A	220	140	ns
Pulsed	5V	125°C	180	60	1000	150	ns

(1) See test circuit; V_{CC} = 30V and I_o = 0.3A.

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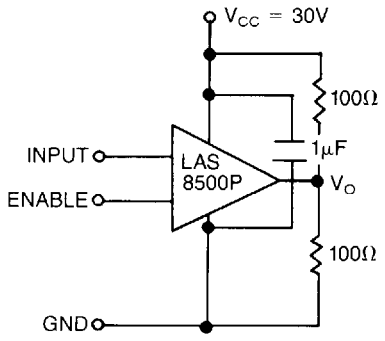
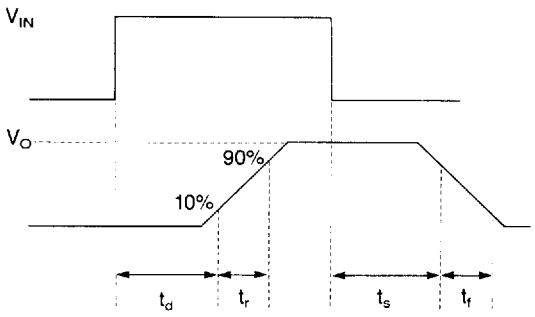
OPERATIONAL DATA

SWITCHING CHARACTERISTICS TEST CIRCUIT



SWITCHING TIMES

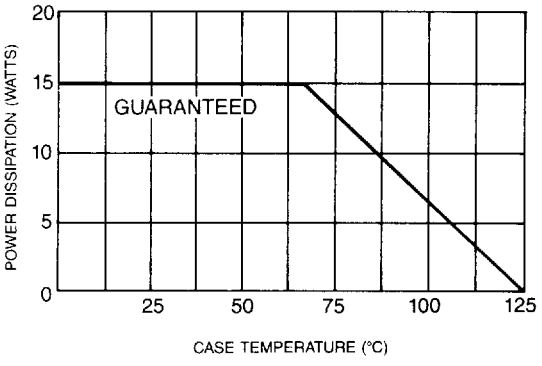


TRUTH TABLE

INPUT		ENABLE	OUTPUT
LAS 8500P	LAS 8501P		
L	H	L	Off (Reset)[1]
H	L	L	Off (Reset)[1]
L	H	H	L
H	L	H	H

(1) Device operation is inhibited, i.e. output is off, when Enable "low" is coupled with an input signal. Device operation is reset after latching thermal shutdown when Enable is momentarily brought "low", if T_J is less than the thermal shutdown value.

POWER DERATING



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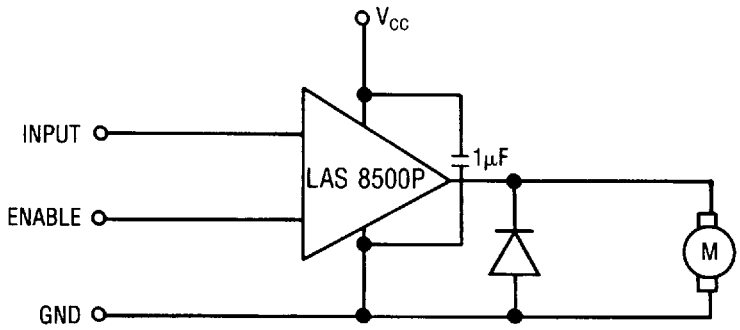
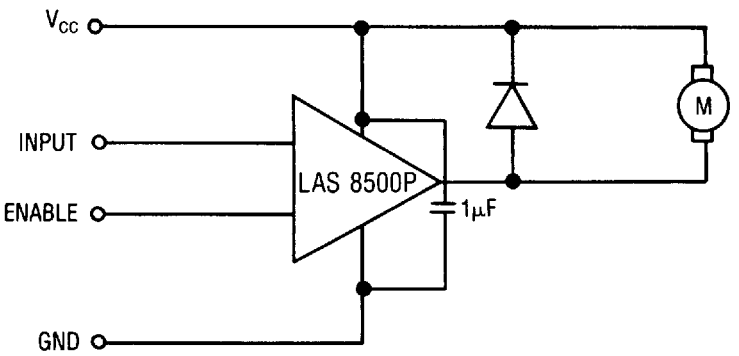
TYPICAL APPLICATIONS

BI-STATE MOTOR DRIVE[1,2]



$$P_D = 0.035\ V_{CC} + I_o\left[3\ (D.C.) + \left(\frac{t_r + t_f}{2\tau}\right)V_{CC}\right]$$

BI-STATE MOTOR DRIVE[2,3]



$$P_D = 0.035\ V_{CC} + I_o\left[2\ (D.C.) + \left(\frac{t_r + t_f}{2\tau}\right)V_{CC}\right]$$

(1) When an inductive load is connected between the V_O terminal and ground, the external sink diode must be added when the output current exceeds 1 amp. This insures pulse width modulation to rated output current.
(2) D.C. = duty cycle
τ = period
(3) When the load is connected between V_O and V_{CC}, and the output current exceeds 1 amp, the external source diode is recommended to lower power dissipation.

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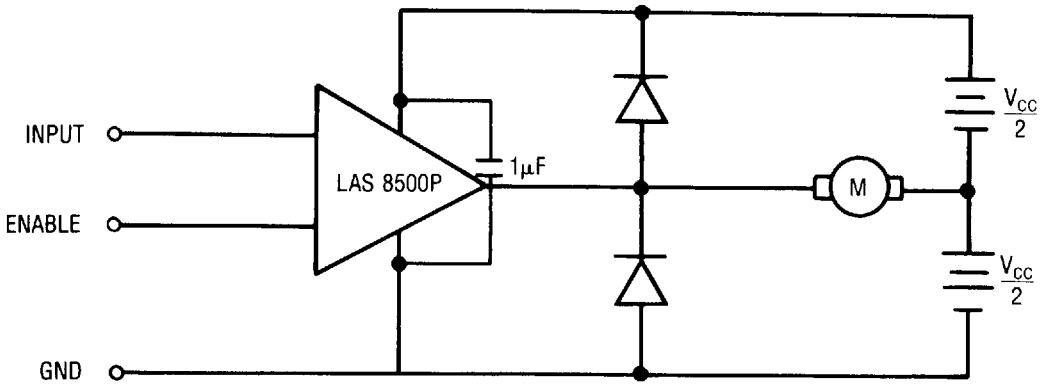
TYPICAL APPLICATIONS

TRI-STATE MOTOR DRIVE USING SPLIT SUPPLY[1]

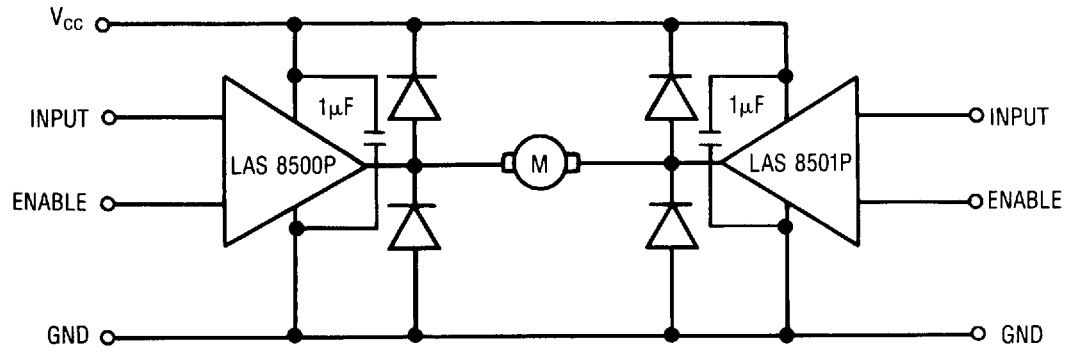


$$P_D = 0.035\ V_{CC} + I_O\left[2\ (D.C.) + \left(\frac{t_r + t_f}{2\tau}\right)V_{CC}\right], \text{ when D.C. } < 50\%$$

$$P_D = 0.035\ V_{CC}, \text{ when D.C. } = 50\%$$

$$P_D = 0.035\ V_{CC} + I_O\left[3\ (D.C.) + \left(\frac{t_r + t_f}{2\tau}\right)V_{CC}\right], \text{ when D.C. } > 50\%$$

TRI-STATE MOTOR DRIVE USING SINGLE SUPPLY[2]



(1) D.C. = duty cycle
τ = period
(2) See power dissipation equations for split supply motor drive.

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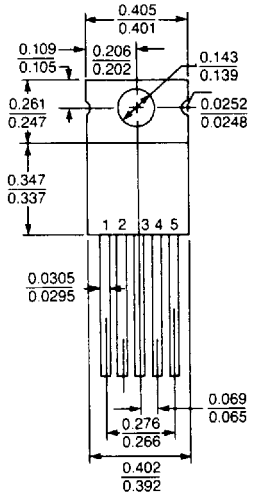
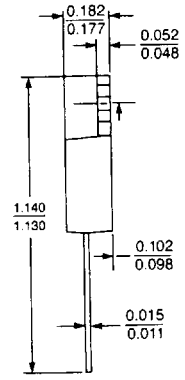
DEVICE OUTLINE

(Front View)



(Side View)



1 – V_{CC}
2 – Input
3 – GND
4 – V_O
5 – Enable
Tab is GND

NOTE: All dimensions are in inches.